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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,405	KIM ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-15, 20-52, 55, and 58-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the admitted prior art, Belopolsky et al (U.S. Patent No. 5,999,400), and Hochgraef et al. (U.S. Patent No. 6,809,913).

Referring to claim 1: The admitted prior art discloses a cable with a conductor set (figure 1). The admitted prior art discloses that each cable has a different characteristic in effecting the data transmission (Specification, page 4, last 2 paragraphs, and page 5, 1st paragraph). Each cable's characteristic is the claimed cable data. The admitted prior art does not disclose the claimed memory and the claimed circuitry.

Belopolsky discloses a cable connector with electronic components coupled to at least one conductor of the conductor set (abstract, figure 1); Belopolsky's electronic components are

the claimed circuitry. Belopolsky's electronic component includes resistors (figure 1, structures 36 and 37), which are analog memories. Belopolsky discloses that it is known to improve electromagnetic compatibility by reducing electromagnetic interference (column 1, lines 9-17), and Belopolsky teaches one to equipment the modular plug with integral component for improving performance or adjusting the capabilities of electronic equipment. Although Belopolsky teaches one to integrate the network cable connector with electronic component for the purpose of managing the electromagnetic interference, Belopolsky does not explicitly disclose that the memory storing any characteristic data.

Hochgraef discloses a cable with a memory module (figures 1-2). Hochgraef discloses that each electronic device has different characteristic values (column 1, lines 22-24, 31-32, and 35-37), and such characteristic has its effect on the signal communication. Hochgraef teaches one to store transmission characteristic related information in a memory of the cable. Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing characteristic values (column 2, lines 48-50), which effect the signal communication, in a memory located within the cable. Although Hochgraef does not explicitly disclose an embodiment that the cable memory stores the cable's characteristic values, Hochgraef teaches one to store any transmission characteristic related information in a memory of the cable (column 1, last paragraph), and Hochgraef further states that it will be obvious that the same may be varied in many ways and not to be regarded as a departure from the spirit and scope of the invention (column 3, 3rd paragraph). Hence, one skilled in the computer art will store the cable information into the cable memory since Hochgraef teaches each electronic device has different characteristic values in

effecting the signal communication, and Hochgraef further teaches storing such information in the cable memory.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teachings of Belopolsky and Hochgraef onto the admitted prior art because Belopolsky teaches one to improve performance or to adjust the capabilities of electronic equipment with a cable modular plug with integral circuitry and Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing communication characteristic values (column 2, lines 48-50) in a memory located within the cable.

Referring to claim 2: Belopolsky discloses a serial device (figure 1, structures 34, 35, 36, 37, and 38), and the serial device includes the circuitry.

Referring to claim 3: Belopolsky discloses resistors (figure 1, structures 36 and 37), which are analog memories and elements of the serial device.

Referring to claim 4: The admitted prior art discloses the I2C interface (Specification, page 4, line 1) and Hochgraef discloses an EEPROM (column 2, line 1), which is a read-only memory.

Referring to claim 5: Belopolsky discloses that the memory is distinct from but coupled to the serial device (figure 1).

Referring to claim 6: The admitted prior art discloses the I2C interface (Specification, page 4, line 1) and Hochgraef discloses an EEPROM (column 2, line 1), which is a read-only memory.

Referring to claim 7: Belopolsky discloses that the cable includes two connectors, the conductor set is coupled between the connectors, and the serial device is included in one of the connectors (figure 1).

Referring claims 8-10: Belopolsky discloses light emitting diodes (LED, figure 1, structure 34), which is the claimed at least one radiation-emitting element. Belopolsky's means to drive the LED is equivalent to the claimed second serial device, and the LED is for responding to signals received on at least one conductor of the conductor set.

Referring to claim 11: The LED blinks in response to signals received.

Referring to claims 12-13: The LED emits light in response to the connection status of the cable; the connection status is a specific signal activity.

Referring to claim 14: Since the cable has at least two connectors, Belopolsky's first cable connector has a first LED, which is the claimed first radiation-emitting element; and Belopolsky's second cable connector has a second LED, which is the claimed second radiation-emitting element. Belopolsky's means to drive the first LED is equivalent to the claimed first serial device and the means to drive the second LED is equivalent to the claimed second serial device.

Referring to claim 15: The admitted prior art discloses that it is known to equip the serial link with cryptographic key set and to execute a verification operation including transmitting at least one cryptographic key of the key set over at least one conductor of the conductor set (Specification, page 2, last paragraph, page 3, first paragraph, figure 1). Both the admitted prior art and Belopolsky explicitly discloses a cable, but none discloses a secure cable. Hochgraef discloses a cable with a memory storing the data related to the signal transmission from the

attached device (column 1, lines 22-24, 31-32, 35-37, and 47-51). Hochgraef teaches that it is known to re-allocate the transmission related data from the attached device to the cable (column 1, lines 47-51). Hence, the cable is a secure cable when adapting Hochgraef's teaching to reallocate the cryptographic information from the attached device as disclosed in the admitted prior art to the cable's memory.

Referring to claim 20: Belopolsky's electronic component includes resistors (figure 1, structures 36 and 37), which are analog memories.

Referring to claim 21: The admitted prior art discloses that frequency-dependent attenuation is one of the factors effecting the signal transmitting (Specification, page 4, 4th paragraph).

Referring to claim 22: The admitted prior art discloses that the conductor set includes at least one conductor pair for differential signal transmission (figure 1) and EMI-related coefficients (Specification, page 4, 4th paragraph).

Referring to claim 23: The admitted prior art discloses that the conductor set includes a first conductor subset (figure 1, structure 22, Channels 0-2) configured for data transmission from a transmitter coupled to the cable to a receiver coupled to the cable, and a second conductor subset (figure 1, structure 22, Analog line) configured for serial communication between the transmitter and the receiver.

As stated above, the admitted prior art does not disclose any circuitry within the cable. Belopolsky discloses serial circuitries located on each one of the cable's conductors (figure 1); Belopolsky teaches one to improve performance or reduce EMI with these circuitries (column 2, lines 14-17). Since Belopolsky's circuitries are located at each one of the cable's conductors,

which are the serial communication medium between the transmitter and the receiver, and Belopolsky's circuitries are to improve performance or to reduce EMI, Belopolsky's circuitry is said to respond to the data request by asserting the accessed data serially to at least one conductor of the conductor subset

Referring to claim 24: The admitted prior art discloses Display Data Channel lines (Specification, page 2, lines 15-16).

Referring to claim 25: The admitted prior art discloses a cable with a conductor set (figure 1). The admitted prior art discloses that each cable has a different characteristic in effecting the data transmission (Specification, page 4, last 2 paragraphs, and page 5, 1st paragraph). Each cable's characteristic is equivalent to the claimed cable guide information. The admitted prior art does not disclose a subsystem coupled to at least one conductor of the conductor set, and configured to respond to a change in state of at least one conductor of the conductor set by asserting cable guide information.

Belopolsky discloses a cable connector with electronic components coupled to at least one conductor of the conductor set (abstract, figure 1). Belopolsky's electronic components are the claimed circuitry. Belopolsky discloses that it is known to improve electromagnetic compatibility by reducing electromagnetic interference (column 1, lines 9-17), and Belopolsky teaches one to equipment the modular plug with integral circuitry for improving performance or adjusting the capabilities of electronic equipment. Belopolsky does not explicitly disclose that the subsystem asserts any information in response of a change in state of at least one conductor of the conductor set.

Hochgraef discloses a cable with a memory module (figures 1-2). Hochgraef discloses that each attached device on the cable has different characteristic values (column 1, lines 22-24, 31-32, and 35-37), and such characteristic has its effect on the signal communication. Hochgraef discloses that the memory of the cable stores these characteristics and the cable asserts the stored information to respond to a change in state of at least one conductor of the conductor set (column 1, line 15). Hochgraef teaches one to store transmission characteristic related information in a memory of the cable. Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing characteristic values (column 2, lines 48-50), which effect the signal communication, in a memory located within the cable.

Both Belopolsky and Hochgraef disclose reducing the electromagnetic interference. Hochgraef discloses that each electronic device has different characteristic values (column 1, lines 22-24, 31-32, and 35-37), such that when the cable inserts into a device, which is a change in the state, the Belopolsky and Hochgraef's mechanism for reducing the electromagnetic interference will be activated. The initialization of such mechanism is to manage the electromagnetic interference by factoring the characteristic values of the attached device/cable, which is equivalent to the asserting the cable guide information.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teachings of Belopolsky and Hochgraef onto the admitted prior art because Belopolsky teaches one to improve performance or to adjust the capabilities of electronic equipment with a modular plug with integral components and Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing signal

communication related characteristic values (column 2, lines 48-50) in a memory located within the cable.

Referring to claim 26: Belopolsky discloses light emitting diodes (LED, figure 1, structure 34), which is the claimed at least one radiation-emitting element. Belopolsky's means to drive the LED is equivalent to the claimed circuitry, and the LED is for responding to signals received from the attached device on at least one conductor of the conductor set. Since LED responses to signal received from the attached device, Belopolsky's means to drive the LED is configured to determine and to response the change in connectivity status of the at least one conductor whether a device is coupled to the cable and to cause the LED to emit indicative of necessary information in response to determining that a device is coupled to the cable.

Referring to claim 27: Belopolsky discloses light emitting diodes (LED, figure 1, structure 34), which is the claimed at least one radiation-emitting element.

Referring to claim 28: The admitted prior art discloses different types of devices with different protocols, such as TMDS and DVI (Specification, page 2). Belopolsky discloses light emitting diodes (LED, figure 1, structure 34), which is the claimed at least one radiation-emitting element. Belopolsky's means to drive the LED is equivalent to the claimed circuitry, and the LED is for responding to signals received from the attached device on at least one conductor of the conductor set. Since the LED responses to signal received from the attached device, Belopolsky's means to drive the LED is configured to determine and to response the change in connectivity status of the at least one conductor whether a device is coupled to the cable. Furthermore, the LED emits radiation indicative of the cable guide information in response to

determining that a device of a specific type is coupled to the cable when adapting Belopolsky's LED practice onto the TMDS and DVI as disclosed in the admitted prior art.

Referring to claim 29: Belopolsky discloses light emitting diodes (LED, figure 1, structure 34), which is the claimed at least one radiation-emitting element.

Referring to claim 30: The admitted prior art discloses different types of devices with different protocols, such as TMDS and DVI (Specification, page 2). Belopolsky discloses light emitting diodes (LED, figure 1, structure 34), which is the claimed at least one radiation-emitting element. Since each cable has at least two connectors, the first LED located at the first connector is the claimed first radiation-emitting element and the second LED located at the second connector is the claimed second radiation-emitting element, and the means to drive the first LED is equivalent to the claimed first serial device and the means to drive the second LED is equivalent to the claimed second serial device. Since the LED responses to signal received from the attached device, Belopolsky's means to drive the LED is configured to determine and to response the change in connectivity status of the at least one conductor whether a device is coupled to the cable. Furthermore, the LED emits radiation indicative of the cable guide information in response to determining that a device of a specific type is coupled to the cable when adapting Belopolsky's LED practice onto the TMDS and DVI as disclosed in the admitted prior art.

Referring to claim 31: The admitted prior art discloses a cable with a conductor set (figure 1). The admitted prior art discloses that each cable has a different characteristic in effecting the data transmission (Specification, page 4, last 2 paragraphs, and page 5, 1st

paragraph). Each cable's characteristic is the claimed cable data. The admitted prior art does not disclose the claimed memory and the claimed circuitry.

Belopolsky discloses a cable connector with electronic components coupled to at least one conductor of the conductor set (abstract, figure 1), and Belopolsky's electronic component includes resistors (figure 1, structures 36 and 37), which are analog memories. Belopolsky discloses that it is known to improve electromagnetic compatibility by reducing electromagnetic interference (column 1, lines 9-17), and Belopolsky teaches one to equipment the modular plug with integral component for improving performance or adjusting the capabilities of electronic equipment. Belopolsky does not explicitly disclose that the memory storing any characteristic data.

Hochgraef discloses a cable with a memory module (figures 1-2). Hochgraef discloses that each attached device on the cable has different characteristic values (column 1, lines 22-24, 31-32, and 35-37), and such characteristic has its effect on the signal communication. Hochgraef teaches one to store transmission characteristic related information in a memory of the cable. Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing characteristic values (column 2, lines 48-50), which effect the signal communication, in a memory located within the cable.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teachings of Belopolsky and Hochgraef onto the admitted prior art because Belopolsky teaches one to improve performance or to adjust the capabilities of electronic equipment with a modular plug with integral components and Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing

characteristic values (column 2, lines 48-50), which effect the signal communication, in a memory located within the cable.

Referring to claim 32: The admitted prior art discloses performing the equalization (Specification, page 5, 1st paragraph).

Referring to claim 33: The admitted prior art discloses a transmitter (figure 1).

Referring to claim 34: The admitted prior art discloses determining pre-emphasis values for use in applying pre-emphasis to the content data (Specification, page 5, 1st paragraph). Furthermore, the admitted prior art discloses that each cable has a different characteristic in effecting the data transmission (Specification, page 4, last 2 paragraphs, and page 5, 1st paragraph). Each cable's characteristic is the claimed cable data. As stated above, the admitted prior art does not disclose a cable with a memory for providing the cable data for use in applying pre-emphasis.

Hochgraef discloses a cable with a memory module (figures 1-2). Hochgraef discloses that each attached device on the cable has different characteristic values (column 1, lines 22-24, 31-32, and 35-37), and such characteristic has its effect on the signal communication. Hochgraef teaches one to store transmission characteristic related information in a memory of the cable. Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing communication related characteristic values (column 2, lines 48-50) in a memory located within the cable.

Referring to claims 35 and 37: The disclosures of the admitted prior art, Belopolsky, and Hochgraef are stated above; furthermore, the admitted prior art discloses a receiver and a cable coupled between the receiver and the transmitter (figure 1). The admitted prior art further

discloses that a receiver or a transmitter is configured to equalize data received over the cable from the transmitter in accordance with at least one equalization parameter (Specification, page 5, 1st paragraph). The admitted prior art discloses that each cable has a different characteristic in effecting the data transmission (Specification, page 4, last 2 paragraphs, and page 5, 1st paragraph). Each cable's characteristic is the claimed cable data. As stated above, the admitted prior art does not disclose a cable with a memory for providing the cable data for setting at least one said equalization parameter.

Hochgraef discloses that the memory of the cable stores the signal transmission related characteristics and the cable asserts the stored information to respond to a change in state of at least one conductor of the conductor set (column 1, line 15), which is equivalent to the claimed configuring to use at least some of the cable data received from the cable to set at least one said equalization parameter.

Referring to claims 36 and 38: The arguments for claims 35 and 37 apply; furthermore, Hochgraef discloses that a release is set according to the data received regarding the circuit breaker (column 1, lines 26-28). Hochgraef's release is equivalent to the claimed receiver and Hochgraef's transmitter is equivalent to the claimed transmitter.

Referring to claim 39: The disclosures of the admitted prior art, Belopolsky, and Hochgraef are stated above; furthermore, the admitted prior art discloses that the conductor set includes a first conductor subset (figure 1, structure 22, Channels 0-2) configured for data transmission from a transmitter coupled to the cable to a receiver coupled to the cable, and a second conductor subset (figure 1, structure 22, Analog line) configured for serial communication between the transmitter and the receiver.

As stated above, the admitted prior art does not disclose any circuitry within the cable. Belopolsky discloses serial circuitries located on each one of the cable's conductors (figure 1); Belopolsky teaches one to improve performance or reduce EMI with these circuitries (column 2, lines 14-17). Since Belopolsky's circuitries are located at each one of the cable's conductors, which are the serial communication medium between the transmitter and the receiver, and Belopolsky's circuitries are to improve performance or to reduce EMI, Belopolsky's circuitry is said to respond to the data request by asserting the accessed data serially to at least one conductor of the conductor subset

Referring to claim 40: The admitted prior art also discloses a second device, wherein the cable is coupled between the device and the second device (figure 1). The admitted prior art further discloses the conductor set includes Display Data Channel lines for serial communication between the device and the second device (Specification, page 2, lines 15-16).

Referring to claim 41: Belopolsky discloses a serial device (figure 1, structures 34, 35, 36, 37, and 38), and the serial device includes the circuitry.

Referring to claim 42: Belopolsky discloses resistors (figure 1, structures 36 and 37), which are analog memories and elements of the serial device.

Referring to claim 43: The admitted prior art discloses the I2C interface (Specification, page 4, line 1) and Hochgraef discloses an EEPROM (column 2, line 1), which is a read-only memory.

Referring to claim 44: Belopolsky discloses that the memory is distinct from but coupled to the serial device (figure 1).

Referring to claim 45: The admitted prior art discloses the I2C interface (Specification, page 4, line 1) and Hochgraef discloses an EEPROM (column 2, line 1), which is a read-only memory.

Referring to claim 46: Belopolsky discloses that the cable includes two connectors, the conductor set is coupled between the connectors, and the serial device is included in one of the connectors (figure 1).

Referring claims 47-48: Belopolsky discloses light emitting diodes (LED, figure 1, structure 34), which is the claimed at least one radiation-emitting element. Belopolsky's means to drive the LED is equivalent to the claimed serial device, and the LED is for responding to signals received on at least one conductor of the conductor set.

Referring to claim 49: The disclosures of the admitted prior art, Belopolsky, and Hochgraef are stated above; furthermore, the prior art discloses a receiver and a transmitter, and the cable is coupled between the receiver and the transmitter (figure 1). As stated above, the admitted prior art does not disclose any circuitry within the cable. Belopolsky discloses serial circuitries located on each one of the cable's conductors (figure 1); Belopolsky teaches one to improve performance or reduce EMI with these circuitries (column 2, lines 14-17). Since LED responses to the signal received from the conductors, and the conductors are the serial communication medium between the transmitter and the receiver, Belopolsky's means to drive the LED is configured to generate signals for driving the LED in response to commands received from at least one of the transmitter and the receiver on at least one conductor of the conductor set.

Referring to claim 50: The LED blinks in response to signals received.

Referring to claims 51-52: The LED emits light in response to the connection status of the cable; the connection status is a specific signal activity.

Referring to claim 55: The admitted prior art discloses that it is known to equip the serial link with cryptographic key set and to execute a verification operation including transmitting at least one cryptographic key of the key set over at least one conductor of the conductor set (Specification, page 2, last paragraph, page 3, first paragraph, figure 1). Both the admitted prior art and Belopolsky explicitly discloses a cable, but none discloses a secure cable. Hochgraef discloses a cable with a memory storing the data related to the signal transmission from the attached device (column 1, lines 22-24, 31-32, 35-37, and 47-51). Hochgraef teaches that it is known to re-allocate the transmission related data from the attached device to the cable (column 1, lines 47-51). Hence, the cable is a secure cable when adapting Hochgraef's teaching to reallocate the cryptographic information from the attached device as disclosed in the admitted prior art to the cable's memory.

Referring to claim 58: Hochgraef discloses an EEPROM (column 2, line 1), which is a read-only memory.

Referring to claim 59: Belopolsky's electronic component includes resistors (figure 1, structures 36 and 37), which are analog memories.

Referring to claim 60: The admitted prior art discloses that frequency-dependent attenuation is one of the factors effecting the signal transmitting (Specification, page 4, 4th paragraph).

Referring to claim 61: The admitted prior art discloses that the conductor set includes at least one conductor pair for differential signal transmission (figure 1) and EMI-related coefficients (Specification, page 4, 4th paragraph).

4. Claims 16-19 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the admitted prior art, Belopolsky, Hochgraef, and Juan (U.S. Pub No. 2004/0230708).

Referring to claims 16 and 56: The disclosures of the admitted prior art, Belopolsky, and Hochgraef are stated above. Furthermore, the admitted prior art discloses that it is known to equip the serial link with cryptographic key set and to execute a verification operation including transmitting at least one cryptographic key of the key set over at least one conductor of the conductor set (Specification, page 2, last paragraph, page 3, first paragraph, figure 1). Although the admitted prior art discloses that it is a known practice to construct a combined security structure wherein the memory storing the decryption key is coupled with a decryption engine, neither the admitted prior art nor Belopolsky explicitly discloses allocating the combined security structure on the connecting cable.

Hochgraef discloses a cable with a memory storing the data related to the signal transmission from the attached device (column 1, lines 22-24, 31-32, 35-37, and 47-51). Hochgraef teaches that it is known to re-allocate the component of the attached device to the cable (column 1, lines 47-51). Although Hochgraef teaches that it is known to re-allocate the component of the attached device to the cable, none of the prior art, Belopolsky, and Hochgraef explicitly discloses a cable with an executing means.

Juan discloses a connecting cable system with a processor (figure 3, paragraph 23). Juan teaches one to implement a plug-and-play data-transferring scheme between different devices with a cable equipped with a controller including a processor and a memory.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Belopolsky, Hochgraef, and Juan onto the admitted prior art because Belopolsky teaches one to improve performance or to adjust the capabilities of electronic equipment with a modular plug with integral components, Hochgraef teaches one to minimize the plug connection (column 1, lines 47-50) by storing characteristic values (column 2, lines 48-50) in a memory located within the cable, and Juan teaches one to support a plug-and-play data communication scheme by equipping the connecting cable with a processor.

Referring to claims 17 and 19: Hochgraef discloses an EEPROM (column 2, line 1), which is a read-only memory.

Referring to claim 18: Juan discloses a mask ROM (paragraph 23).

Referring to claim 57: The admitted prior art discloses a receiver (figure 1), wherein the cable is coupled between the receiver and the transmitter. The admitted prior art further discloses that the transmitter is configured to perform a verification operation with the receiver including by transmitting at least one cryptographic key over at least one conductor of the conductor set (Specification, page 2, last paragraph, page 3, first paragraph, figure 1).

5. Claims 53-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the admitted prior art, Belopolsky, Hochgraef, and Onsen (U.S. Patent No. 6,473,811).

Referring to claim 53: The disclosures of the admitted prior art, Hochgraef, Belopolsky, and Hochgraef are stated above; none of them explicitly discloses that the transmitter or the receiver includes a LED and a circuit for driving the LED. Onsen discloses a method for display connecting status with the LED light (abstract, figure 6). Onsen teaches one to equip a LED on the receiver to indicate the connection status, and the receiver's means to drive the LED is the claimed circuit. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Onsen's teachings onto the admitted prior art, Belopolsky, and Hochgraef because Onsen enables one to visually determine the serial device's connecting status by equipping the serial device a LED.

Referring to claim 54: The LED emits light in response to the connection status of the cable. The admitted prior art discloses different types of devices with different protocols, such as TMDS and DVI (Specification, page 2), and the LED is for responding to signals received from the attached device on at least one conductor of the conductor set.

Response to Arguments

6. In response to Applicant's assertion that Applicant disagrees that the Application includes any prior art that it is conventional to store cable data of the type recited in claim (Remark, page 12, 4th paragraph): The Office Action as stated above does not argue that the convention stores cable data of the type recited.

7. In response to Applicant's argument that resistor is not an analog memory (Remark, page 12, last paragraph): Resistor is considered as an analog memory. A memory is a device with capability of holding values. Resistor stores an electronic value; thus, it is considered as a

memory. Additional support can be found in Singh (U.S. Patent No. 6,306,718), column 2, lines 10-17).

8. In response to Applicant's argument that the Belopolsky does not disclose or teach the "circuitry of the type recited" (Remark, page 13, 1st paragraph), and Hochgraef does not disclose or teach the cable as claimed (Remark, page 13, 2nd paragraph), and neither prior arts discloses or teaches a memory in a cable or to store cable data or a cable circuitry (Remark, page 13, last paragraph): Belopolsky discloses a cable connector with electronic components coupled to at least one conductor of the conductor set (abstract, figure 1). Belopolsky's electronic components are the claimed circuitry. Belopolsky discloses that it is known to improve electromagnetic compatibility by reducing electromagnetic interference (column 1, lines 9-17), and Belopolsky teaches one to equipment the modular plug with integral component for improving performance or adjusting the capabilities of electronic equipment. Since Belopolsky's electronic component improves the electromagnetic capability, Belopolsky discloses that the circuitry is configured to respond to a data transmission. Although Belopolsky teaches one to integrate the network cable connector with electronic component for the purpose of managing the electromagnetic interference on cable, and it is known that the cable itself also has unique characteristics in effecting the electromagnetic interference, Belopolsky does not explicitly disclose that the memory storing the cable characteristic data. Hochgraef discloses that each electronic device has different characteristic values (column 1, lines 22-24, 31-32, and 35-37), and such characteristic has its effect on the signal communication. Although Hochgraef does not explicitly disclose an embodiment that the cable memory stores the cable's characteristic values, Hochgraef teaches one to store any transmission characteristic related information in a memory of the cable (column

1, last paragraph), and Hochgraef further states that it will be obvious that the same may be varied in many ways and not to be regarded as a departure from the spirit and scope of the invention (column 3, 3rd paragraph). Hence, one skilled in the computer art will store the cable information into the cable memory since Hochgraef teaches each electronic device has different characteristic values in effecting the signal communication, and Hochgraef further teaches storing such information in the cable memory.

9. In response to Applicant's argument that the Specification page 6, 1st paragraph and page 22, 1st paragraph discloses a cable guide information can indicate to what type of device a free end of the cable should be connected (Remark, page 14, 1st paragraph): The quoted Specification does not disclose a cable guide information *indicating* to what *type* of device a free end of the cable should be connected. The quoted Specification only discloses a cable guide information to identify/determine whether a connected device is a proper/appropriate device by particular LED blinking sequence.

10. In response to Applicant's argument that the prior arts on record do not disclose or teach asserting cable guide information (Remark, page 14, 2nd paragraph): Both Belopolsky and Hochgraef disclose reducing the electromagnetic interference. Hochgraef discloses that each electronic device has different characteristic values (column 1, lines 22-24, 31-32, and 35-37), such that when the cable inserts into a device, which is a change in the state, the Belopolsky and Hochgraef's mechanism for reducing the electromagnetic interference will be activated. The initialization of such mechanism is to manage the electromagnetic interference by factoring the characteristic values of the attached device/cable, which is equivalent to the asserting the cable guide information.

Conclusion

11. The prior art made of recorded and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,885,100 to Talend et al.: Talend discloses that it is well known in the computer art to equip a connector equipped with a LED, which that the LED responses to signals received on at least one conductor of the conductor set (column 1, lines 10-20).

U.S. Patent No. 6,311,270 to Challenger et al.: Challenger discloses a hardware a structure of security chip comprising of a memory storing encryption key and a decryption engine for producing decrypted content.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests

to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
April 27, 2006

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